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51 - 60 of about 1,240 for **mos diffusion source drain current shape** - 0.52 sec. (About this page

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51. With contact to **source** or **drain** region of refractory material (e.g., polysilicon, tungsten, or silicide) - Patent ...

... to have a stripe-like **shape** and with a ... reductions in **current** density, in turn, reduce the **source-to-drain** turn on ... Efficient **source**/**diffusion** interconnect, **MOS** transistor and standard ...
With_contact_to_**source**_or_**drain**_region... - 48k - Cached - More from this site - Save

52. Chapter 4 Modeling of the Enclosed Layout Transistor (PDF)

... **Drain** and **Source diffusion**. A. Figure 4.1: ELT **shape**. The transistor ... with. the **drain current** of standard devices with ... output conductance in an **MOS** transistor, right ... The dotted ...
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53. Experiment 4 - **MOS** Device Characterization

Experiment 4 - **MOS** Device Characterization. W.T. Yeung and R.T. Howe. UC Berkeley EE 105. 1.0 Objective. In this experiment, you will find the device parameters for an n-channel MOSFET. ... as follows: (**drain** = PIN3 gate = PIN4 **source** = PIN 5 ... If the width of **diffusion** area is 46.5 m ... the **MOS** enters into the saturation region, the **drain current** should remain ...
...berkeley.edu/ee105/Exp4.fm5.html - 25k - Cached - More from this site - Save

54. Microsoft Word - Vol.3 Table of Contents (PDF)

... Equation for Simulating **Diffusion** in Submicron Device Structures 24 ... Approach to Deriving the DC **Drain-Current** Relationships in ... **Source/Drain** Junctions to Suppress Punchthrough in ...
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55. U.S. Patent: 6025620 - Semiconductor device and method of producing the same - February 15, 2000

... **current** in the junction such as a field edge is large. Therefore, although there was a merit that resistances of the **diffusion** ... of **source/drain** regions in said **MOS** transistor ...
- 69k - Cached - More from this site - Save

56. Cours en ligne - CMOS Design - **MOS** Modeling

CMOS Design > **MOS** Modeling. **MOS** Model 3. The **MOS** model 3 is slightly more complicated than model 1. We show here some of the most important equations. ... **Drain Diffusion**. The lateral **drain diffusion** (LDD) vis a ... **current** is the standby **current** appearing between **drain** and **source** for Vgs=0 ...
/Cours/CMOS/mos_model3.html - 7k - Cached - More from this site - Save

lucy.mrs.org/meetings/spring99/abstractbook/AbstractBookR.html - 242k - Cached - More from this site - Save

58. Quiz answers
... the area including **source diffusion**, **drain diffusion** and poly gate ... pull-up stack whose **shape** factors are 3 * 1.2 * 10 ... a function of programming **current** more than any other parameter ...
www-ee.eng.hawaii.edu/~msmith/ASICs/HTML/Quiz/qzans.htm - 18k - Cached - More from this site - Save

59. Lab 1. **MOS** Device Characterization
ECE-E432 Microelectronics II. Drexel University Electrical & Computer Engineering. Lab 1. - **MOS** Device Characterization. Written by W.T. Yeung and R.T. Howe for UC Berkeley course EE 105. Modified by K. ... as follows: **drain** = PIN 3, gate = PIN 4, **source** = PIN 5 ... Comment on the **shape** of the graph ... the **MOS** enters into the saturation region, the **drain current** should remain ...
www.ece.drexel.edu/courses/ECE-E432/Lab1.**MOS**_Devices.html - 21k - Cached - More from this site - Save

60. United States Patent: 4,829,349
... the **drain current** in a MOSFET is due to thermionic emission from the **source** which ... the height and **shape** of the potential barrier ... of the effective **diffusion** velocity on the ...
www.ee.sunysb.edu/~serge/pat08.html - 36k - Cached - More from this site - Save

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Phase change memory array - Patent 6862214
In order to increase a cell **drive current**, the phase change memory also ... of the phase change cells are separated by shallow **trench isolation** (STI). ...
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N-channel metal oxide semiconductor (**NMOS**) **driver** circuit and ...
forming a shallow **trench isolation** (STI) and a gate on a substrate, ... 1A is a **layout** diagram of an **NMOS driver** circuit according to the present invention; ...
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[5] H. Yamashina and H. Yamada, "An **MOS current** mode logic ... **shaped** CVD-SiO2 **isolation** structure and a BPSG-refilled. **trench**," International Electron ...
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retrograde wells and the use of Shallow **Trench Isolation** (STI). ... the **drive** capability of the **NMOS**. As a result, both the node ...
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The most sensitive parts of an **MOS** transistor from the point of view of the ... increase the node capacitance and the transistor **current drive** capability. ...
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tp_abstracts inline
Other structural parameters such as thickness of **trench** sidewall oxide, ... The paper discussed **NMOS** predope enhanced off-state leakage **current** related to ...
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With **trench isolation**, V. th. falls as W falls due to prop. greater C ... **Current** into the **drive** gate's parasitic diodes and gate overlap (bad) ...
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The evolution of IBM CMOS DRAM technology
A p-**MOS** DRAM array built in an n-well CMOS technology meets these ... As a result of the cell **layout**, the **isolation trench** etch, which is done next, ...

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1 Noise considerations for mixed-signal RF IC transceivers

Sayfe Kiaei, David Allstot, Ken Hansen, Nishath K. Verghese
January 1998 **Wireless Networks**, Volume 4 Issue 1
Publisher: Kluwer Academic Publishers
Full text available: pdf(629.05 KB) Additional Information: full citation, abstract, references, index terms

This paper discusses design trade-offs for mixed-signal radio frequency integrated circuit (RF IC) transceivers for wireless applications in terms of noise, signal power, receiver linearity, and gain. During air wave transmission, the signal is corrupted by channel noise, adjacent interfering users, image signals, and multi-path fading. Furthermore, the receiver corrupts the incoming signal due to RF circuit non-linearity (intermodulation), electronic device noise, and digital switching noi ...

2 Interconnect scaling implications for CAD

Ron Ho, Ken Mai, Hema Kapadia, Mark Horowitz
November 1999 **Proceedings of the 1999 IEEE/ACM international conference on Computer-aided design**
Publisher: IEEE Press
Full text available: pdf(91.68 KB) Additional Information: full citation, abstract, references, citings, index terms

Interconnect scaling to deep submicron processes presents many challenges to today's CAD flows. A recent analysis by Sylvester and Keutzer examined the behavior of average length wires under scaling, and controversially concluded that current CAD tools are adequate for future module-level designs. In our work, we show that average length wire scaling is sensitive to the technology assumptions, although the change in their behavior is small under all reasonable scaling assumptions. H ...

3 Technical reports

SIGACT News Staff
January 1980 **ACM SIGACT News**, Volume 12 Issue 1
Publisher: ACM Press
Full text available: pdf(5.28 MB) Additional Information: full citation

4 Preparing for the future

M. Plazzi, W. Carlson, R. Lucas, M. Schweppe, M. Yanilmaz
July 1989 **ACM SIGGRAPH Computer Graphics , ACM SIGGRAPH 89 Panel Proceedings SIGGRAPH '89**, Volume 23 Issue 5
Publisher: ACM Press
Full text available: pdf(8.64 MB) Additional Information: full citation, abstract, index terms

Welcome to Preparing for the Future, a panel on educational issues in computer graphics. The field of computer graphics education, as no other, combines the disciplines of science and art, and in this sense presents computer graphics instructors in both art and science with some unique problems not faced by their counterparts in other fields.As computer graphics courses become a standard addition in art and science curricula, the way in which we prepare students for this evolutionary field is ch ...

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IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

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1. **Parametric study of latchup immunity of deep trench-isolated, bulk, none**
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